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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,591	10/30/2003	Richard Holzmann	TMS-0002	8315

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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,591	HOLZMANN, RICHARD	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 6/30/2006

2. Claims 1-7 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1, 3, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenguel et al. ("Berenguel") in view of Fallon et al. U.S. Patent No. 6,748,457 ("Fallon").

8. As per claim 1, Berenguel teaches a solid state disk system comprising:

a non-volatile storage media [20 fig. 1];

a memory module [22 fig. 1];

an interface module for communicating with a computer network [24 fig. 1];

control module [30 fig. 1] operatively coupled to the non-volatile storage media, the memory module, and the interface module;

a load priority queue stored by said control module for maintaining a list of data segment requests received by said interface module[col. 11 lines 46-52];

a sequential load map [38 fig. 1]stored by said control module for storing the order in which data segments are copied from said non-volatile storage media to said memory module [col. 8 lines 27-35; col. 14 lines 66];

said control module; during start-up of the solid state disk system, copying data segments from said non-volatile storage media to said memory module [step 100-102-104-106-108-110 fig. 4; col. 11 lines 9-12];

said control module, during start-up of the solid state disk system, checking the load priority queue [col. 11 lines 46-54];

said control module, if data segments are listed in said load priority queue, temporarily stopping said copying of data segments listed in said sequential load map [step 62-56-58-59 fig. 2];

said control module copying the data segments listed in the load priority queue from the non-volatile storage media to said memory module [step 59 (69)-70-72-74 fig. 2];

said control module, after all data segments in said load priority queue have been copied, resuming said copying of data segments listed in said sequential load map [step 74-56 fig. 2].

However, Berenguel does not teaches a sequential load map for storing the order in which data segments are copied from said non-volatile storage media to said memory module during start-up of said solid state disk system; and

said control module; during start-up of the solid state disk system, copying data segments from said non-volatile storage media to said memory module in the order listed in said sequential load map.

Fallon teaches another data storage controllers comprises a cache memory device for storing data that is processed by or transmitted through the data storage controller. Specifically, Fallon teaches a sequential load map [list - 76 fig. 7b; 96 fig. 8b]stored by said control module for storing the order in which data segments are copied from said non-volatile storage media to said memory module during start-up of said solid state disk system [col. 22 lines 34-37; col. 23 lines 40-66, col. 24 lines 1-2];

said control module; during start-up of the solid state disk system, copying data segments from said non-volatile storage media to said memory module in the order listed in said sequential load map [col. 22 lines 51-55; col. 24 lines 3-8].

Berenguel and Fallon are analogous art because they from the same field of endeavor; Cache memory in solid state disk system.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have modified the Berenguel's system with the sequential load map of Fallon to pre-fetch the cache memory with the most frequently used data segments.

The suggestion/motivation for doing so would have been to increases the hit ratio which would improve the performance of the cache device in the solid state disk system.

Therefore, it would have been obvious to combine Berenguel with Fallon to obtain the invention as specified in claim 1.

9. As per claim 3, Berenguel teaches the interface module, upon receiving a read or write request from said computer via a SCISI bus, issues a command to said control module to check the load priority queue [col. 10 lines 17-22; col. 16 lines 46-50].

However, Fallon teaches the data storage controller may be utilized to receive a read or write request from the computer system via well know interface such as SCSI, FiberChannel, or to a network communication channels [col. 6 lines 23-32; col. 10 lines 28-38. Therefore, it would have been obvious to one of ordinary skill in the art to combine Berenguel with Fallon to obtain the invention as specified in claim 3.

10. As per claim 5, The combine teaching of Berenguel and Fallon teach a solid state disk system. As such, Berenguel and Fallon teach the method for operating the solid state disk system.

11. As per claim 6, see discussion in claim 3.

12. As per claim 7, Berenguel et al. do not explicitly teach, upon receiving a data access request form the computer network, the interface module issuing a command to the control module to immediately check the load priority queue. However, this feature is deemed to be inherent to the Berenguel et al. system as col. 10 lines 17-22 shows the system needed to keep

tracks of which pages of blocks have been successfully completely transferred during the process in case the process gets interrupted by a read request from the host because, upon receiving the read request, the control module had to stop the transferring process immediately in order to perform the read request.

13. Claims 2, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berenguel et al. as applied to claim 1, 3 above, and further in view of Yamagami et al. U.S. Patent 5,592,630.

14. As per claim 1, Berenguel et al. teach the memory module is a hard disk cache. Berenguel et al. do not teach the memory module is a RAM module.

Yamagami et al. teach another systems related to a data transfer system having a storage device such as disk having a memory module capable of transferring data at higher speed than the storage device. Specifically, Yamagami et al. teach the memory module is a RAM module [107 fig. 1]. At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the memory module of Berenguel et al. with a RAM module of Yamagami et al. to further accelerate the reading and writing to and from the data storage since it is well know in the art that RAM has a much higher access rate than of the hard disk module.

15. As per claim 4, Yamagami et al teach the control module issuing a notice to said interface module when all data segments listed in the load priority queue have been copied from said non-volatile storage media to said memory module [1207 fig. 14].

Conclusion

16. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran

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